

2018156

by Jonathan Davies

Submission date: 18-Jan-2022 09:16PM (UTC+0000)

Submission ID: 169525327

File name: 16749_Jonathan_Davies_2018156_179500_1138028674.pdf (761.73K)

Word count: 3681

Character count: 15191

45-50

Course: HNC Electrical and Electronic Engineering
Module: SGEE5000 – Electronics II
Assignment Title: Finite State Machines
Name: Jonathan Daffydd Lee Davies
University number: 2018156
Date Submitted: 18/01/2022
Word Count: 1872 words

- ① SOME GOOD RESEARCH WITH IN-TEXT CITATION.
- ② DESIGN METHOD WAS EXPLAINED, SOME K-MAPS WERE GROUPED WRONG.
- ③ CIRCUITS WERE TESTED BUT LOGIC ANALYSER WAS NOT SET UP CORRECTLY FOR ANY OF THEM
- ④ ANALYSIS WAS DIFFICULT AS RESULTS WERE INCOMPLETE.
- ⑤ CONCLUSIONS WERE GOOD WITH CONSIDERATION FOR SUSTAINABILITY.
- ⑥ MODIFICATION NOT ATTEMPTED.

Table of Contents

Introduction	3
Research	4
Design	8
Testing	22
Conclusion	23
Referencing	24
Annex	25

Introduction

Within the following assignment the outcome will be to demonstrate and apply the theory involved in designing complex electronic circuits with the understanding of needs to promote sustainable development. With critical analysis of the design and performance of the complex electronic circuit with adaptation of design to meet new applications.

Research into traffic light systems and the use of FPGA and ASIC designs with comparisons and consideration for improvements in design to aid sustainability will be made. Circuit design of a traffic light system constructed from 3 separate circuits individually designed, constructed and tested before being combined together to create a large functioning circuit.

Research

There are 5 types of traffic signal control pedestrian crossings that have different characteristics, these are Pelican, Puffin, Toucan, Zebra and Pegasus. Each type of signal control has its own characteristics and must comply with the BS 505: 1971.

Pelican crossing – the pelican crossing is a pushbutton that starts a sequence once pressed by a pedestrian. The crossing uses far-side pedestrian signal heads and a flashing amber/flashing green crossing period, of a fixed duration, which is demanded solely by push button (Department of transport, 1995) The timings of the pelican crossing are determined by the location and conditions of the site with consideration with things like the length of the crossing, traffic and pedestrian use. The table below shows the sequences and the signals with the timings for each period. The pelican crossing is the only traffic system that has an amber flashing sequence. (Driving school Beckenham, n.d.)

Table 4 PELICAN CROSSINGS - OPERATIONAL CYCLE & TIMINGS

PERIOD	SIGNALS SHOWN		TIMINGS (Seconds)
	TO PEDESTRIANS	TO VEHICLES	
A	Red Standing Figure (wait)	Steady Green (proceed if way is clear)	20-60 (fixed) 6-60 (VA)
B	Red Standing Figure	Steady Amber (stop unless not safe to do so)	3 (Mandatory)
C	Red Standing Figure	Steady Red (stop, wait behind Stop line on carriageway)	1 to 3
D	Green Walking Figure with audible signal if provided (cross with care)	Steady Red	4 to 7 (in some circumstances plus 2)
E	Flashing Green Figure (do not start to cross)	Steady Red	0 or 2
F	Flashing Green Figure	Flashing Amber (give way to pedestrians on the crossing - they have priority)	6 to 18
G	Red Standing Figure	Flashing Amber	1 or 2

(Department of transport, 1995) Fig 1.1

Zebra crossing – The zebra crossing is a crossing that has a continuous flashing amber beacons to make drivers aware that there is a crossing and to be alert in case of pedestrians waiting to cross. The flashing rates, the photometric performance of globes and construction and electrical requirements are set out in BS 873(16) (Department of transport, 1995).

1201NI (05/01) Regulations, Sign Classification and Standards

Puffin crossing – The Puffin crossing is similar to the pelican crossing with the addition of a pedestrian sensor that can extend the crossing time if pedestrians are still on the walkway. This achieved in 2 ways by using kerb side sensors and on crossing sensors. The use of near-side pedestrian signal heads and an extendable all-red crossing period which is instigated by a push button request accompanied by a pedestrian detector demand. It is intended that the Puffin operational cycle will become the standard form of pedestrian crossing at stand-alone crossings and junctions. (Department of transport, 1995)

The table below shows the sequences and timings of a puffin crossing

Table 6 PUFFIN CROSSINGS - OPERATIONAL CYCLE & TIMINGS

PERIOD	SIGNALS SHOWN		TIMINGS (Seconds)
	TO PEDESTRIANS	TO VEHICLES	
1	Red Standing Figure (Wait)	Green (proceed if way is clear)	20-60 (fixed) 6-60 (VA)
2	Red Standing Figure	Amber (stop unless not safe to do so)	3
3	Red Standing Figure	Red (stop, wait behind Stop line on carriageway)	1 to 3
4	Green Walking Figure with audible signal if provided (cross with care)	Red	4 to 9
5	Red Standing Figure (do not start to cross)	Red	1-5
6	Red Standing Figure	Red	0-22 (pedestrian extendable period)
7	Red Standing Figure	Red	0-3 (only appears on a maximum change if pedestrians are still being detected)
8	Red Standing Figure	Red	0-3 (only appears at a pedestrian gap change)
9	Red Standing Figure	Red with Amber (stop)	2

(Department of transport, 1995) Fig 1.2

Toucan crossings – Are similar as puffin and pelican crossings but also allow cyclists to cross as well as pedestrians. Toucan crossings are typically found in environments near parks and cycle paths and lanes. Like the puffin crossing the toucan crossing does not have a flashing amber sequence. (Driving school Beckenham, n.d.)

The table below shows the sequences and timings of a toucan crossing

Table 8 TOUCAN CROSSINGS - OPERATIONAL CYCLE & TIMINGS

PERIOD	SIGNALS SHOWN		TIMINGS (Seconds)
	TO PEDESTRIANS	TO VEHICLES	
I	Red Standing Figure (Wait)	Green (proceed if way is clear)	20-60 (fixed) 6-60 (VA)
II	Red Standing Figure	Amber (stop unless not safe to do so)	3 (mandatory)
III	Red Standing Figure	Red (stop, wait behind stop line on carriageway)	1 to 3
IV	Green Walking Figure with audible signal if provided (cross with care)	Red	4 to 7
V	Black-out - no signal shown (Do not start to cross)	Red	3 (fixed period)
VI	Black-out	Red	0 to 22 pedestrian extendable period)
VII	Black-out	Red	0-3 (only appears on a maximum change if pedestrians are still being detected)
VIII	Red	Red	1-3
IX	Red Standing Figure	Red with Amber (stop)	2

Fig 1.3

Pegasus crossing – Pegasus crossings or equestrian crossings are the least common types of crossings and allow horses and their riders to cross. There are 2 push buttons set at different heights. One at pedestrian level and one at horse rider's level. The Pegasus crossing acts like a puffin crossing. (Driving school Beckenham, n.d.)

Different technologies can be used to implement control circuitry of the traffic light system these include FPGA - Field Programmable Gate Array and ASIC – Application specific integrated circuit.

FPGA is a functionally customisable programable circuit with digital logic circuitry. With the benefits of requiring less power and faster operation due to being programmed specifically for a desired application. (Maths Works, 1994-2022) FPGA's contain adaptive logic modules (ALM) and logic elements (LE) which are connected through programmable interconnects. (Trochimiuk, 2021) Unlike other types of CPU's and microcontrollers the blocks within the FPGA create a physical array of logic gates that can be customised. (Trochimiuk, 2021)

ASIC is an electronic circuit that consists of many integrated circuits (ICs) which are interconnected together to perform a particular function (Brooks, 2019) and is typically used for a product that will have a large run such as washing machines, mobile phones and other appliances with digital circuits. As the cost of ASIC design is high the use of ASIC systems is typically high-volume products as the larger quantities of the ASIC builds lower the price. (Electronics Notes, n.d.)

Both FPGA and ASIC circuits can be used together within the process of designing and implementing the control process of the traffic light system as the FPGA allows the design and simulation of the circuit and allows the ability to troubleshoot with the ability to amend errors. The FPGA works in the way of a prototype and once complete and working as expected the circuit can be finalised before being passed on to the ASIC production in order to singularly or mass produce the circuit design. (Trochimiuk, 2021)

FPGA is a low cost reprogrammable and can be changed as required from error correction to circuit redesign, which is an advantage however, because of this there is very little security in terms of intellectual property protection and can be compromised via USB or other transfer methods. ASIC is a high cost hard programmed circuit with the information, once on the circuit, is secure and cannot be removed. This protects the intellectual property and allows the product to be sold onwards. The disadvantage of ASIC means that the circuit cannot be changed and if any errors are present, they can not be resolved

Modern electronic components help promote sustainability and safety this has been shown with the transition from a 3-bulb system behind coloured lenses, used initially with traffic lights, to multiple coloured LED's. The LED requires less power, less maintenance and have a longer life span than a light bulb. If the light bulb was to stop working, then the traffic lights will not be displaying correctly and could cause an accident. Whereas if a LED bulb or even a number fail the light will still be visible and will remain safe until LEDs are replaced. To further promote sustainability the use of solar panel or wind turbine can be used to power the traffic light system.

SOME GOOD RESEARCH, MORE DIAGRAMS WOULD HELP.

Circuit design

Specification

To design a sequential circuit for a traffic light system there are several stages to follow. The progress is split into 3 separate parts before combining. The first stage is to compile a truth table for the 0 to 5 sequence. This is followed by the state diagrams, state table and the Karnaugh maps. The final stage is the circuit design.

State Diagram

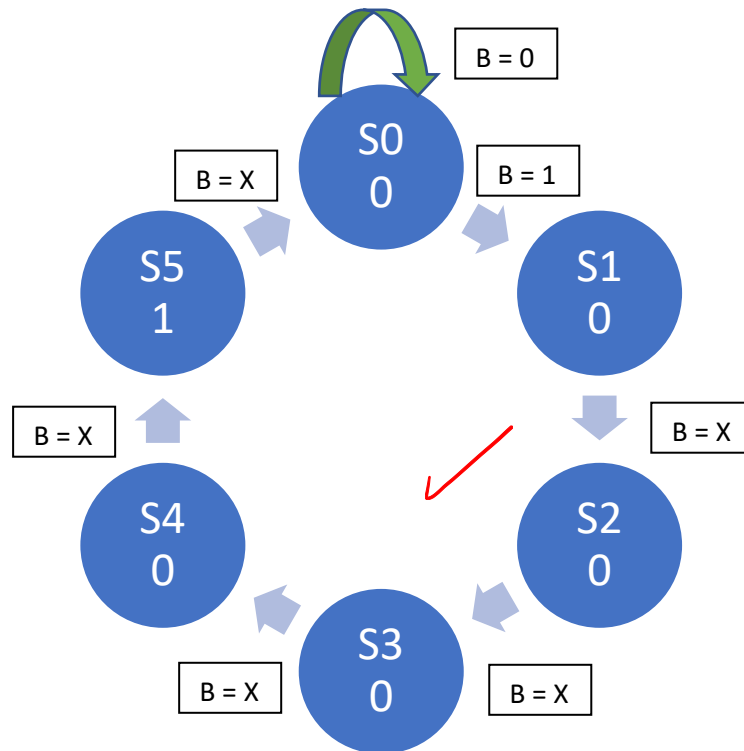


Fig 2.1

State Table

Current State	Next state		Current			Next B = 0			Next B = 1			Output
			QA	QB	QC	QA ⁺	QB ⁺	QC ⁺	QA ⁺	QB ⁺	QC ⁺	W
S0	S0	S1	0	0	0	0	0	0	0	0	1	0
S1	S2	S2	0	0	1	0	1	0	0	1	0	0
S2	S3	S3	0	1	0	0	1	1	0	1	1	0
S3	S4	S4	0	1	1	1	0	0	1	0	0	0
S4	S5	S5	1	0	0	1	0	1	1	0	1	0
S5	S0	S6	1	0	1	0	0	0	0	0	0	1
S6	X	X	1	1	0	X	X	X	X	X	X	X
S7	X	X	1	1	1	X	X	X	X	X	X	X

Karnaugh Maps

USE SUBSCRIPT /
SUPERSCRIPT

Q_A^+

$BQ_A \backslash Q_B Q_C$	00	01	11	10
00	0	0	1	0
01	1	0	X^1	X^1
11	1	0	X^1	X^1
10	0	0	1	0

$$Q_A^+ = QAQ\bar{C} + QBQC$$

$BQ_A \backslash Q_B Q_C$	00	01	11	10
00	0	1	0	1
01	0	0	X^0	X^1
11	0	0	X^0	X^1
10	0	1	0	1

$$Q_B^+ = QBQ\bar{C} + Q\bar{A}Q\bar{B}QC$$

SHOW GROUPS.

$BQ_A \backslash Q_B Q_C$	00	01	11	10
00	0	0	0	1
01	1	0	X^0	X^1
11	1	0	X^0	X^1
10	1	0	0	1

$$Q_C^+ = QBQ\bar{C} + QAQ\bar{C} + BQ\bar{C}$$

$Q_A \backslash Q_B Q_C$	00	01	11	10
00	0	0	0	0
01	0	1	X^1	X^0

$$W = QAQC$$

Circuit Design

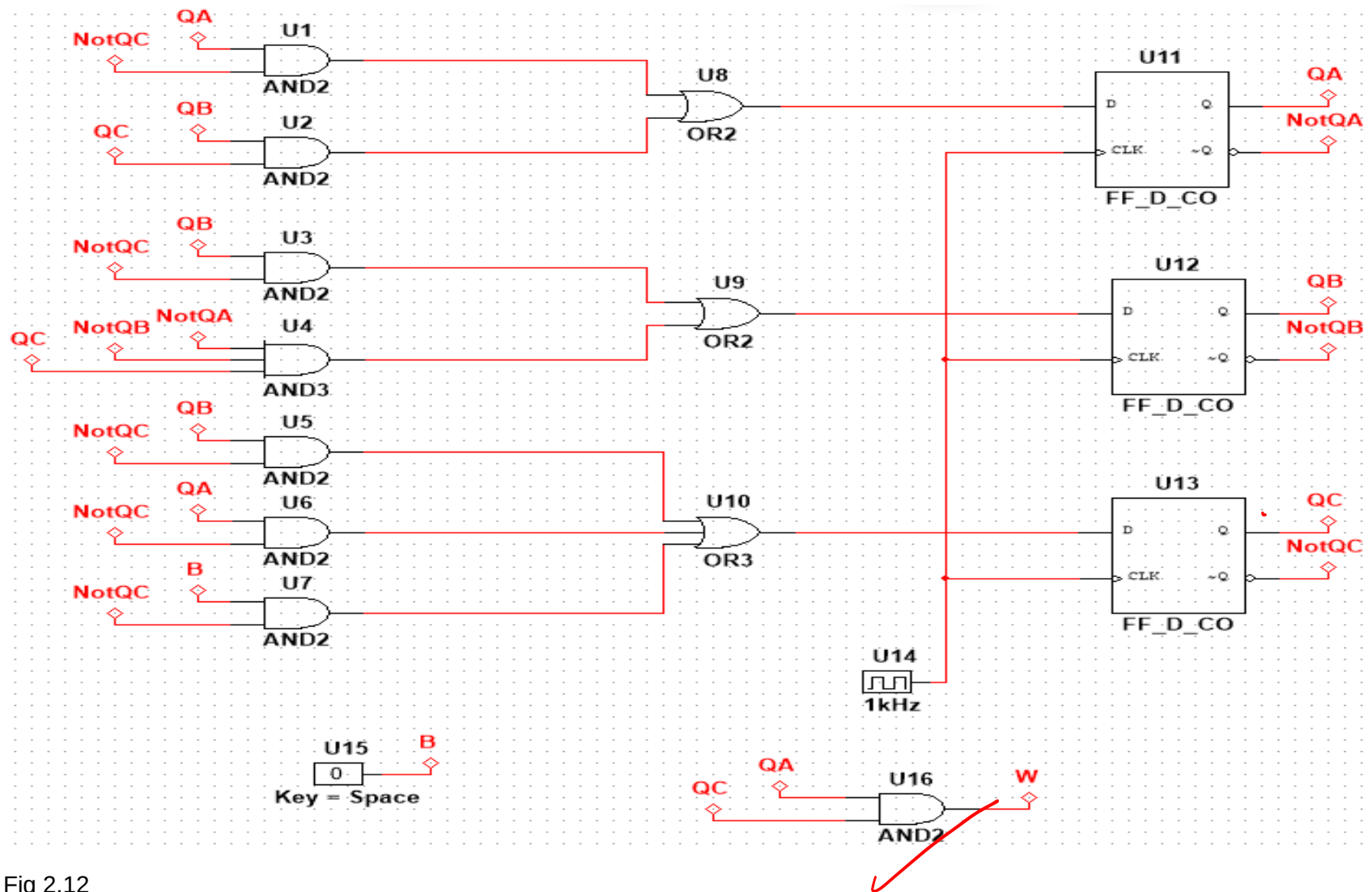


Fig 2.12

15 second timer

Specification

The first stage is to compile a truth table for the 15 second timer sequence. This is followed by the state diagrams, state table and the Karnaugh maps. The final stage is the circuit design. The Karnaugh maps are larger and more complex within the 15 second timer circuit.

State Diagram

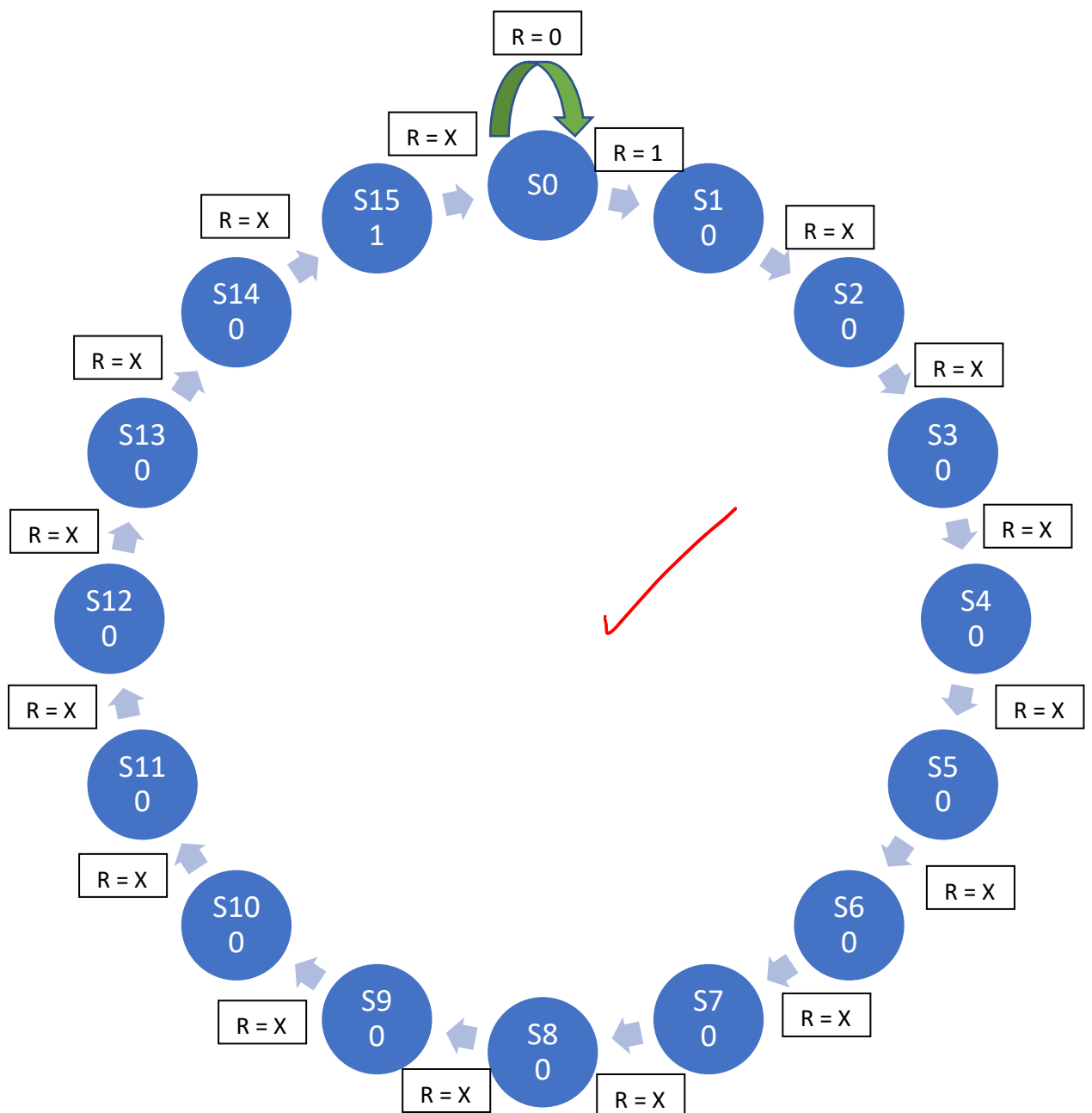


Fig 2.2

15 Second timer state table

Current State	Next state		Current				R = 0				R = 1				Output T
	R = 0	R = 1	QA	QB	QC	QD	QA ⁺	QB ⁺	QC ⁺	QD ⁺	QA ⁺	QB ⁺	QC ⁺	QD ⁺	
S0	S0	S1	0	0	0	0	0	0	0	0	0	0	0	1	0
S1	S2	S2	0	0	0	1	0	0	1	0	0	0	1	0	0
S2	S3	S3	0	0	1	0	0	0	1	1	0	0	1	1	0
S3	S4	S4	0	0	1	1	0	1	0	0	0	1	0	0	0
S4	S5	S5	0	1	0	0	0	1	0	1	0	1	0	1	0
S5	S6	S6	0	1	0	1	0	1	1	0	0	1	1	0	0
S6	S7	S7	0	1	1	0	0	1	1	1	0	1	1	1	0
S7	S8	S8	0	1	1	1	1	0	0	0	1	0	0	0	0
S8	S9	S9	1	0	0	0	1	0	0	1	1	0	0	1	0
S9	S10	S10	1	0	0	1	1	0	1	0	1	0	1	0	0
S10	S11	S11	1	0	1	0	1	0	1	1	1	0	1	1	0
S11	S12	S12	1	0	1	1	1	1	0	0	1	1	0	0	0
S12	S13	S13	1	1	0	0	1	1	0	1	1	1	0	1	0
S13	S14	S14	1	1	0	1	1	1	1	0	1	1	1	0	0
S14	S15	S15	1	1	1	0	1	1	1	1	1	1	1	1	0
S15	S0	S0	1	1	1	1	0	0	0	0	0	0	0	0	1

Karnaugh maps and Boolean equations

R = 0					R = 1				
AB\CD	00	01	11	10	AB\CD	00	01	11	10
00	0	0	0	0	00	0	0	0	0
01	0	0	1	0	01	0	0	1	0
11	1	1	0	1	11	1	1	0	1
10	1	1	1	1	10	1	1	1	1

$$QA^+ = A\bar{B} + A\bar{C} + A\bar{D} + \bar{A}BCD$$

R = 0					R = 1				
AB\CD	00	01	11	10	AB\CD	00	01	11	10
00	0	0	1	0	00	0	0	1	0
01	1	1	0	1	01	1	1	0	1
11	1	1	0	1	11	1	1	0	1
10	0	0	1	0	10	0	0	1	0

$$QB^+ = B\bar{C} + B\bar{D} + \bar{B}CD$$

R = 0					R = 1				
AB\CD	00	01	11	10	AB\CD	00	01	11	10
00	0	1	0	1	00	0	1	0	1
01	0	1	0	1	01	0	1	0	1
11	0	1	0	1	11	0	1	0	1
10	0	1	0	1	10	0	1	0	1

$$QC^+ = \bar{C}D + C\bar{D}$$

R = 0					R = 1				
AB\CD	00	01	11	10	AB\CD	00	01	11	10
00	0	0	0	1	00	0	0	0	1
01	1	0	0	1	01	1	0	0	1
11	1	0	0	1	11	1	0	0	1
10	1	0	0	1	10	1	0	0	1

$QD^+ = C\bar{D} + \bar{D}R + B\bar{D} + A\bar{D}$

T = ABCD

Circuit Design

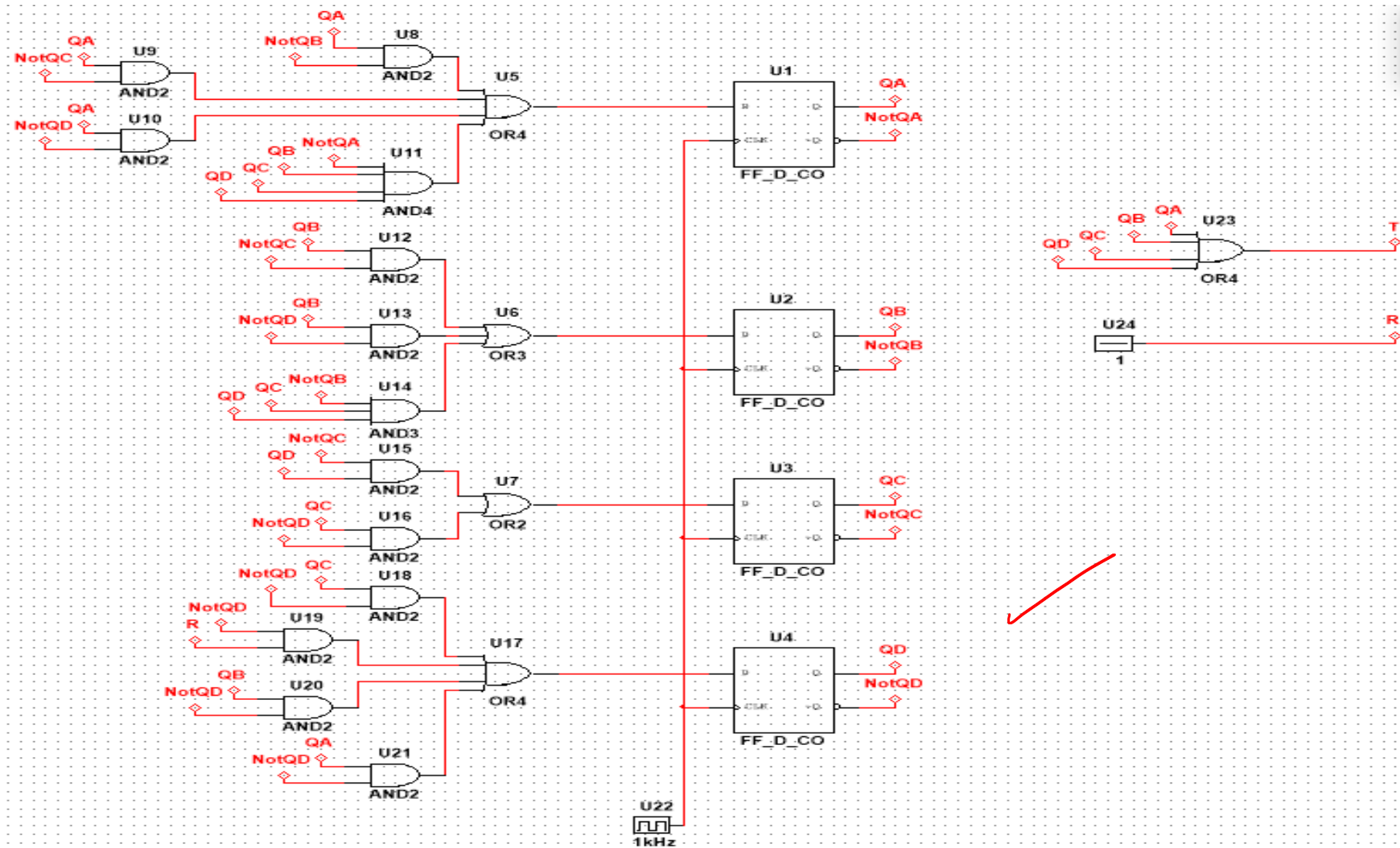


Fig 2.22

Red Amber Green (RAG) output

Specification

The final stage is to compile a truth table for the RAG controller sequence. This is followed by the state diagrams, state table and the Karnaugh maps. The sequence is simpler than the 15 second timer sequence and contains repeated states and variable.

State diagram

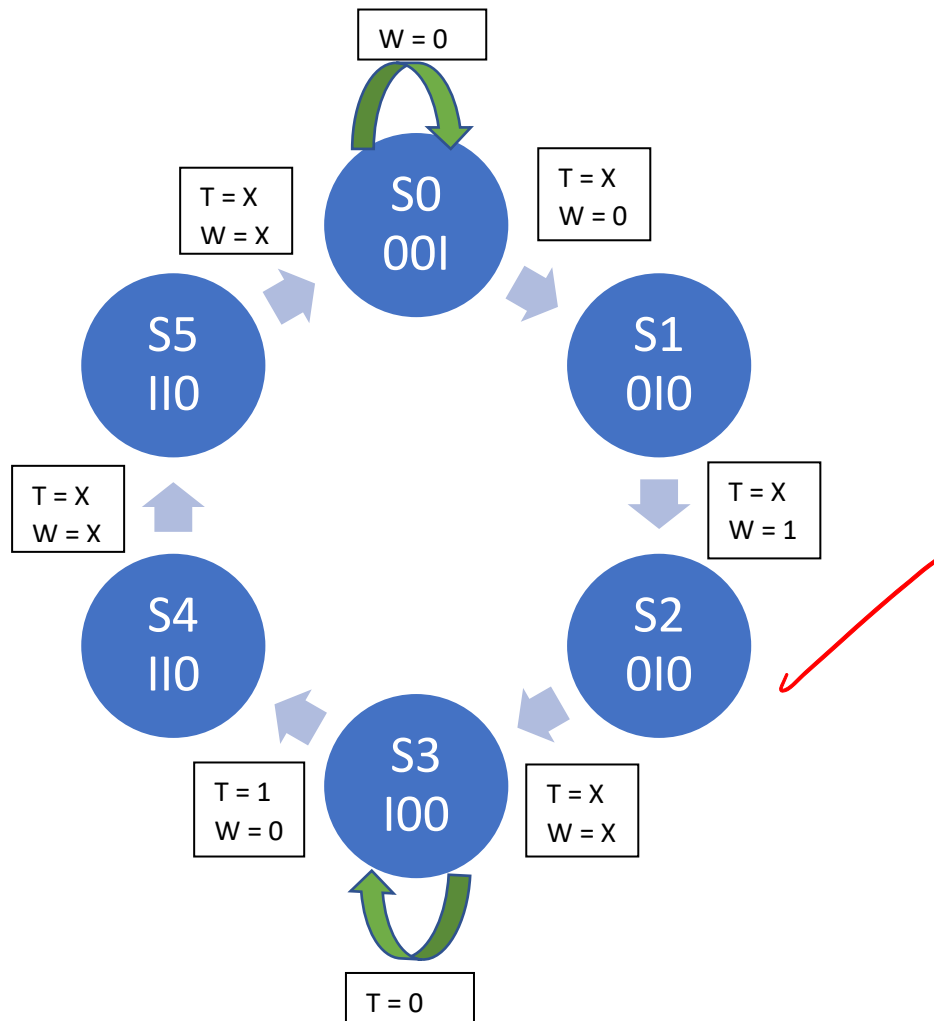


Fig 2.3

Karnaugh maps and Boolean equations

W = 0					W = 1				
TQA\QBQC	00	01	11	10	TQA\QBQC	00	01	11	10
00	0	0	0	0	00	0	0	0	0
01	1	0	X	X ¹	01	1	0	X	X ¹
11	1	0	X ¹	X ¹	11	1	0	X ¹	X ¹
10	0	0	1	0	10	0	0	1	0

$$QA^+ = QA\bar{Q}\bar{C} + TQBQC$$

W = 0					W = 1				
TQB\QBQC	00	01	11	10	TQB\QBQC	00	01	11	10
00	0	1	1	1	00	0	1	1	1
01	0	0	X ¹	X ¹	01	0	0	X ¹	X ¹
11	0	0	X	X ¹	11	0	0	X	X ¹
10	0	1	0	1	10	0	1	0	1

$$QB^+ = QB\bar{Q}\bar{C} + \bar{T}QB + \bar{Q}\bar{A}\bar{Q}\bar{B}QC$$

W = 0					W = 1				
TQB\QBQC	00	01	11	10	TQB\QBQC	00	01	11	10
00	0	0	1	1	00	1	1	1	1
01	1	0	X ¹	X ¹	01	1	0	X ¹	X ¹
11	1	0	X	X ¹	11	1	0	X	X ¹
10	0	0	0	1	10	1	1	0	1

$$QC^+ = QA\bar{Q}\bar{C} + QB\bar{Q}\bar{C} + W\bar{Q}\bar{C} + \bar{T}QB$$

RAG Output truth table

Current State	W=0		W=1		W = 0 [T=0]			W=0 [T=1]			W=1 [T=0]			W=1 [T=1]			Output		
	T= 0	T= 1	T = 0	T = 1	QA	QB	QC	QA ⁺	QB ⁺	QC ⁺	QA ⁺	QB ⁺	QC ⁺	QA ⁺	QB ⁺	QC ⁺	R	A	G
S0	S0	S0	S1	S1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
S1	S2	S2	S2	S2	0	1	0	0	1	0	0	1	0	0	0	1	0	1	0
S2	S3	S3	S3	S3	0	1	1	0	1	1	0	1	1	0	0	1	0	1	0
S3	S3	S4	S3	S4	0	1	1	1	0	0	0	1	1	0	1	0	1	0	0
S4	S5	S5	S5	S5	1	0	1	1	0	1	1	0	1	1	0	1	1	1	0
S5	S0	S0	S0	S0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
S6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
S7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Circuit design

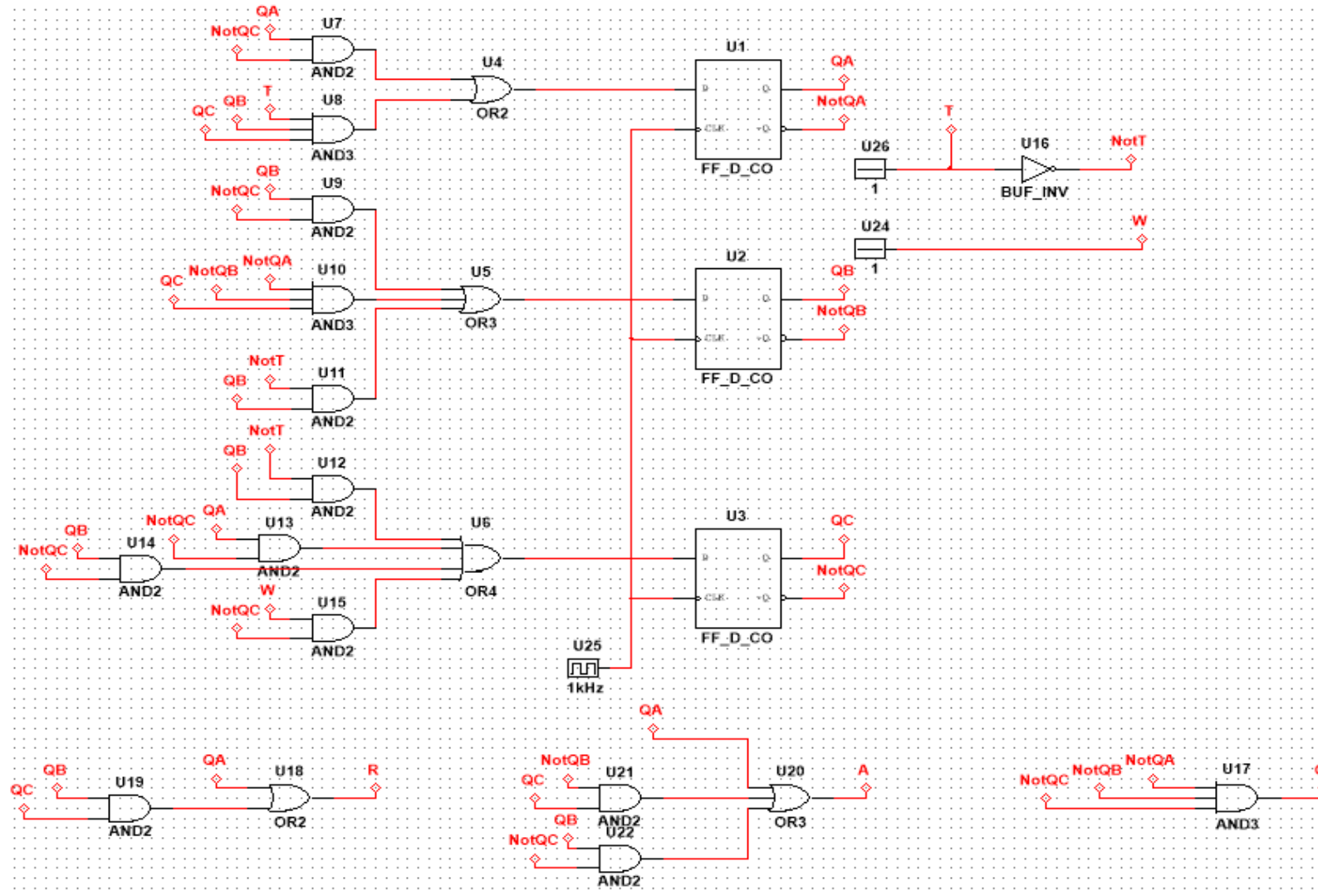


Fig 2.32

Pelican crossing circuit

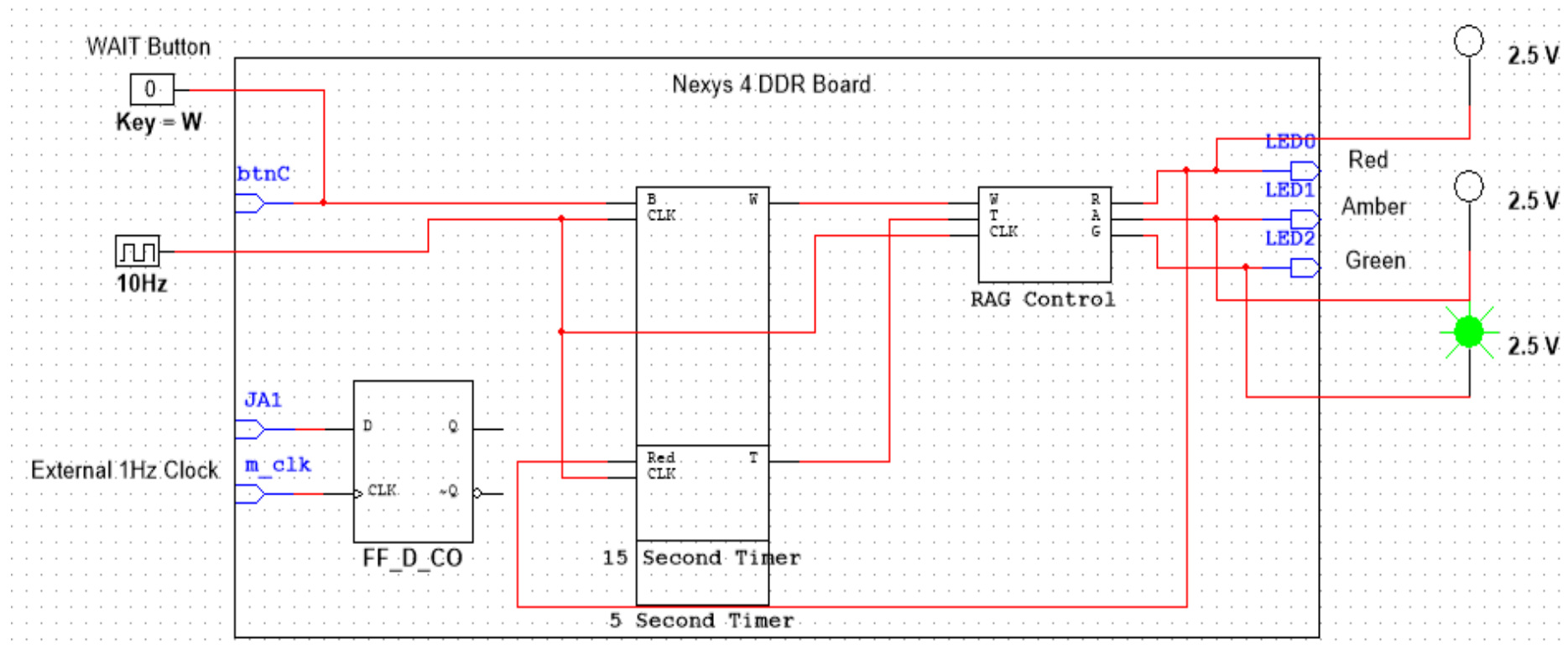


Fig 2.4

Testing results

Logic analysers placed on each individual circuit which simulate individual parts of the pelican crossing sequence. The 5 second counter analyser is placed on the circuit outputs fig 5.1 with the parameters of the analyser set fig 5.2 and when run the analyser graph fig 5.3 shows the sequence following the state diagram as designed in fig 2.1 with $W = 1$ once the count has reached S5. This circuit is the waiting sequence from when the pedestrian waits for the flow of traffic to stop when the traffic lights move through the sequence.

The 15 second counter is placed on circuit outputs and the inverted buffer fig 5.4 with parameters set 5.5 with the simulation run the analyser graph fig 5.6 shows the sequence of the state diagram designed in fig 2.2 with $R=1$ then $T = 1$ sequence continues until $T= 0$ when S15 is reached. As the sequence for the 15 second is larger and more complex there are more analyser connections. The connections of W and T remain at a flat high level due to the simulated digital high input that represent the functioning circuit. This circuit is the activated timer sequence of the pedestrian crossing the road.

The final individual circuit tested is the RAG circuit where the analyser placed in fig 5.7 with the set parameters of fig 5.8 displays the graphs fig 5.9, fig 6.0 and fig 6.1. This shows the sequence from the state diagram 2.3 where the sequence of the traffic light system is constructed. The sequence of the pelican crossing is Green, Amber, Amber, Red, Red Amber, Green.

After testing each individual circuit by placing components such as high digital inputs and a clock to simulate a final circuit the final circuit is constructed and tested. The complete circuit fig 2.4 contains the sub circuits with the substituted components removed and replaced with the digital inputs and outputs. The analyser is placed on the red, amber and green lights and the sequence is run where the green light is activated, with the button then pressed to activate the RAG sequence. The analyser graphs fig 6.2, fig 6.3 and fig 6.4 show the pelican crossing sequence working as a complete circuit. The complete circuit operates fully automated and uses internal clocks and timers.

Conclusion

The result and operation of the designed and constructed circuit in the outlined specification of a finite state machine that will control a pelican crossing worked as required where a pedestrian activates the crossing by pressing the wait (W) button to start the sequence of traffic light changes that would control the flow of traffic. The initial design is made of 3 separate PLD circuits that is combined to create the final circuit. The final circuit is fully automatic and runs from an internal clock with interval timers. The circuit mirrors the pelican crossing with puffin crossing sequence as outlined through in researched theory in fig 1.2. As the pelican crossing features a flashing amber sequence and does not contain an amber and red with amber sequence as shown in fig 1.1. As the puffin crossing is safer as it allows longer to cross by delaying the sequence with the use of sensors it would be more beneficial to alter the initial design of the 5 second counter to include a sensor that detects the pedestrian and interrupts the sequence if no pedestrian is detected. The new design will improve safety as well the flow of traffic if the pedestrian leaves the area and is the desired method of crossing outlined by the department of transport.

In order to promote sustainability within the system the use of LED's in the physical application of the traffic light system helps reduce the cost and usage of electricity of the system and increases the longevity of the lights. The safety is improved as there are several LED's in clusters if one or two fail then the light can continue without disrupting traffic and pedestrian flow.

With the system designed and tested and in a working order the circuit design could be implemented as an ASIC. As the cost of ASIC can be high with small production orders the constant improvement of old traffic light systems and the installation of new will benefit from the sales and implementation for the circuit. ASIC are compact and use very little power to operate this helps with continued sustainability improvements. Intellectual property is protected and the information and design on the ASIC boards cannot be compromised or copied.

References

Brooks, E., 2019. *A guide to Asic design*. [Online]

Available at: <https://www.system-to-asic.com/blog/what-is-asic-design/#whatis>

[Accessed 15 Jan 2022].

Department of transport, 1995. *Design of pedestrian crossings*. [Online]

Available at:

https://assets.publishing.service.gov.uk/government/uploads/system/uploads/attachment_data/file/330214/ltn-2-95_pedestrian-crossings.pdf

[Accessed 15 December 2021].

Driving school Beckenham, n.d. *Pedestrian crossings*. [Online]

Available at: [https://www.driving-school-beckenham.co.uk/pedestriancrossings.html#:~:text=Toucan%20\(Two%20can%20cross\)%20crossings,%20two%20can'%20cross\).&text=Toucan%20crossings%20do%20not%20have,phase%20like%20normal%20traffic%20lights.](https://www.driving-school-beckenham.co.uk/pedestriancrossings.html#:~:text=Toucan%20(Two%20can%20cross)%20crossings,%20two%20can'%20cross).&text=Toucan%20crossings%20do%20not%20have,phase%20like%20normal%20traffic%20lights.)

[Accessed 02 January 2021].

Electronics Nots, n.d. *What is ASIC*. [Online]

Available at: https://www.electronics-notes.com/articles/electronic_components/programmable-logic/what-is-an-asic-application-specific-integrated-circuit.php

[Accessed 18 Jan 2022].

Maths Works, 1994-2022. *FGA Programming*. [Online]

Available at: <https://uk.mathworks.com/discovery/fpga-programming.html>

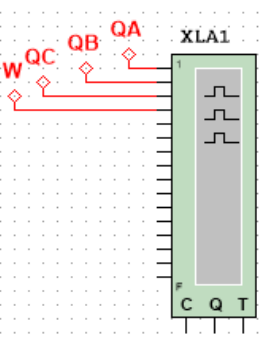
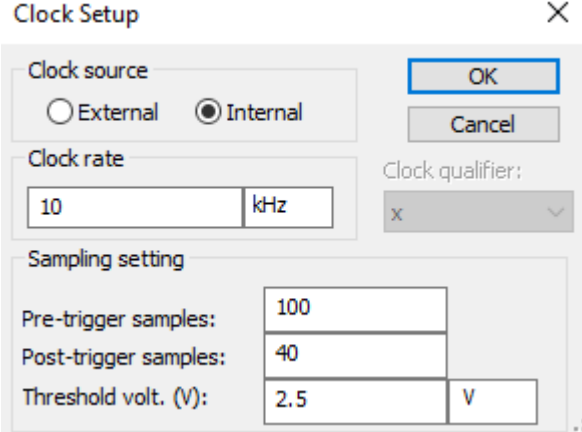
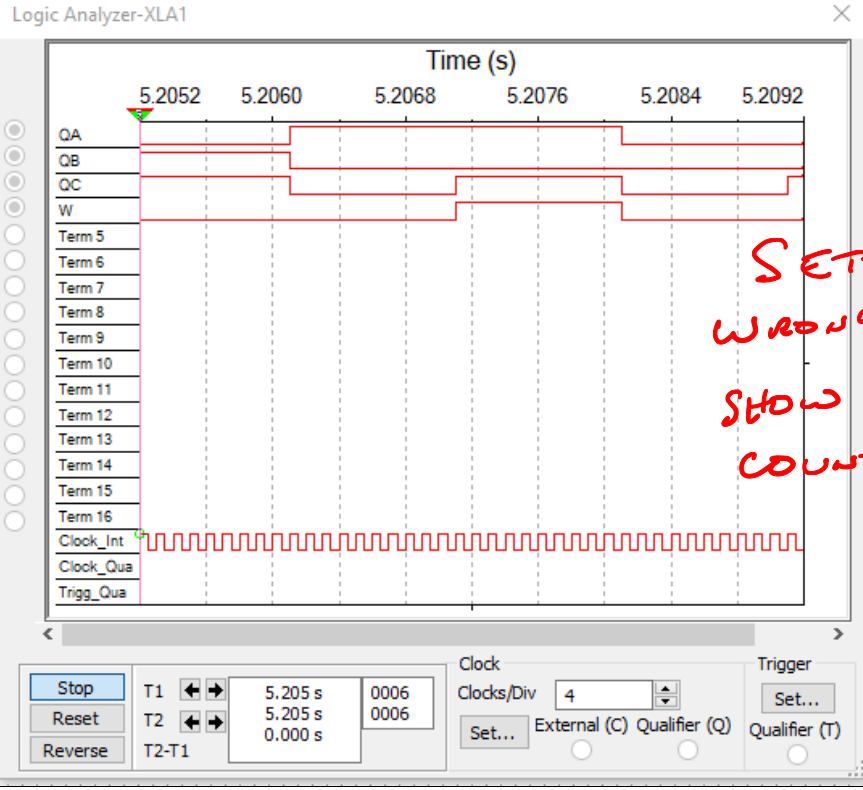
[Accessed 16 Jan 2022].

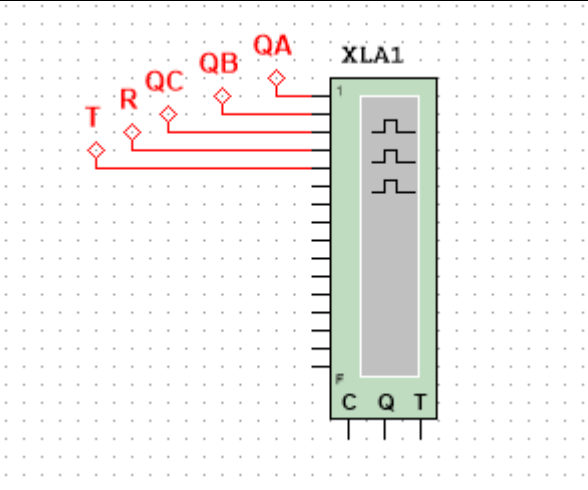
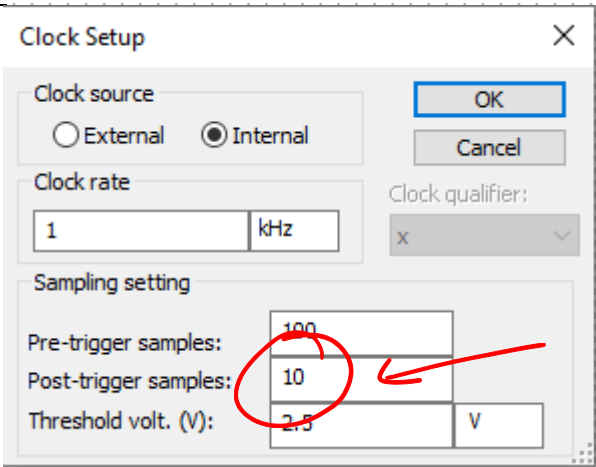
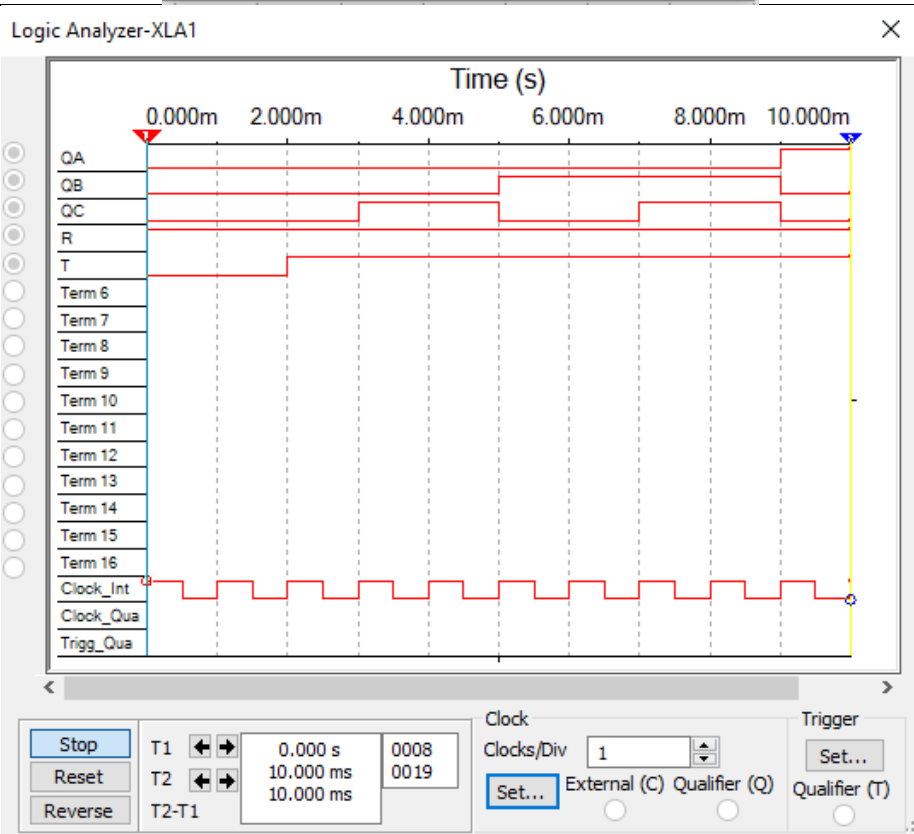
Trochimiuk, M., 2021. *FGPA Programming what is it? and where can it be used?*. [Online]

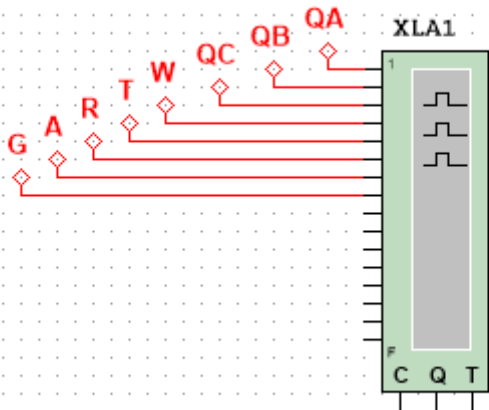
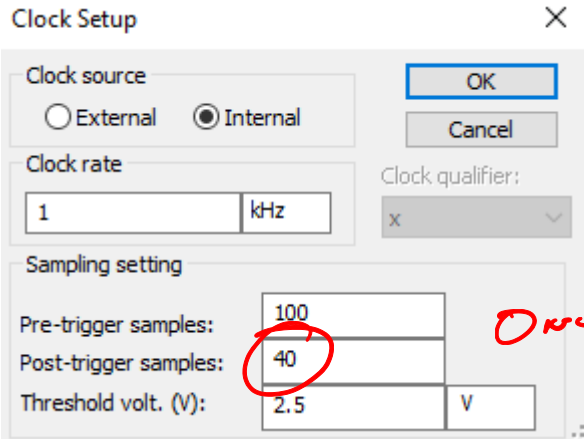
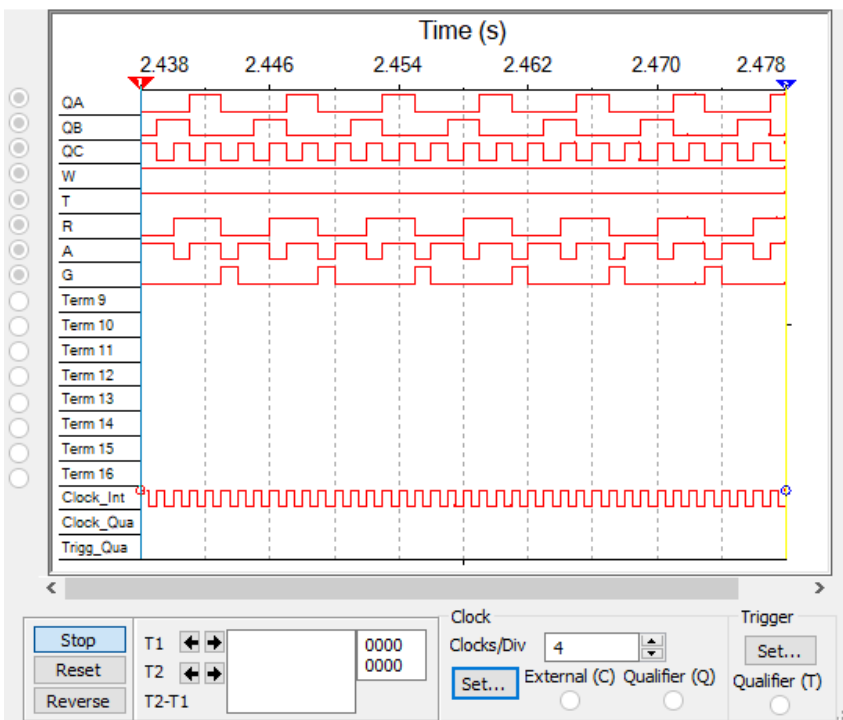
Available at: <https://codilime.com/blog/FPGA-programming-how-it-works-and-where-it-can-be-used/>

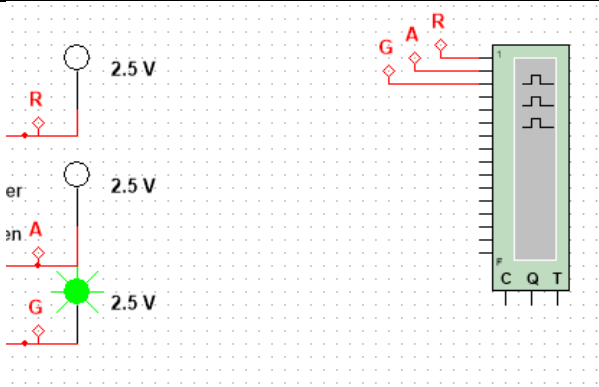
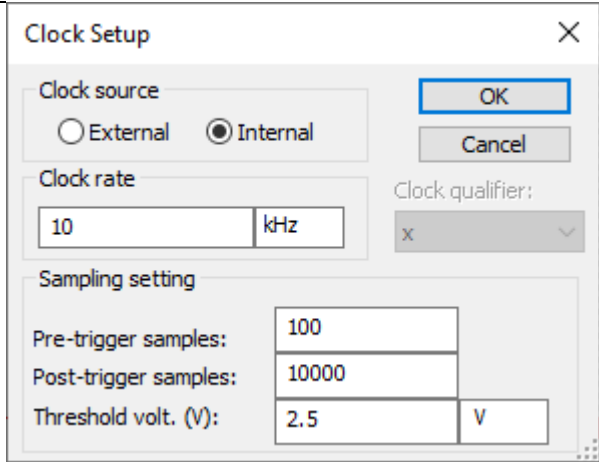
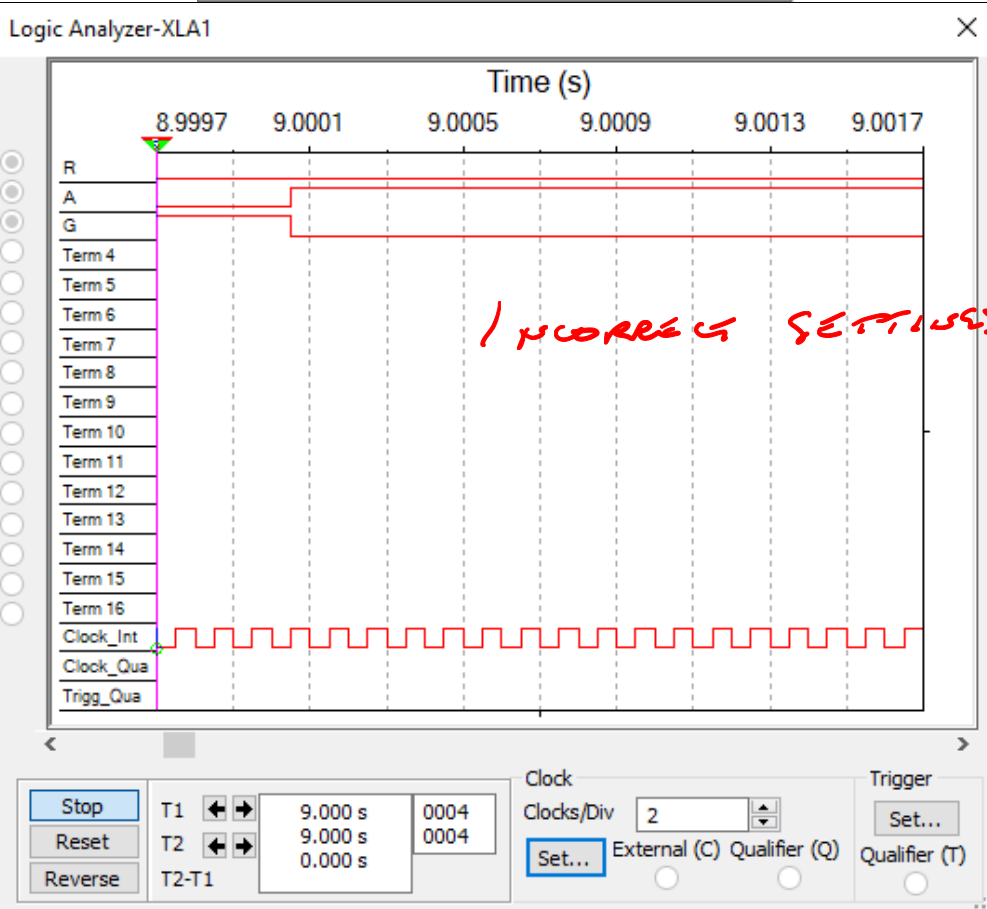
[Accessed 16 Jan 2022].

Annex

5 second counter analyser		Fig 5.1
5 second counter clock setup		Fig 5.2
5 second counter analyser graph		Fig 5.3

15 second counter analyser		Fig 5.4
15 second counter clock setup	 <i>NEEDS TO BE AT LEAST 20.</i>	Fig 5.5
15 second counter graph		Fig 5.6

RAG analyser		Fig. 5.7
RAG clock setup	 Only needs 10	Fig. 5.8
RAG analyser graph		Fig.5.9

Traffic light analyser		Fig: 6
Traffic light clock setup		Fig 6.1
Traffic light analyser graph	 1 incorrect settings	Fig 6.2

Traffic light analyser graph

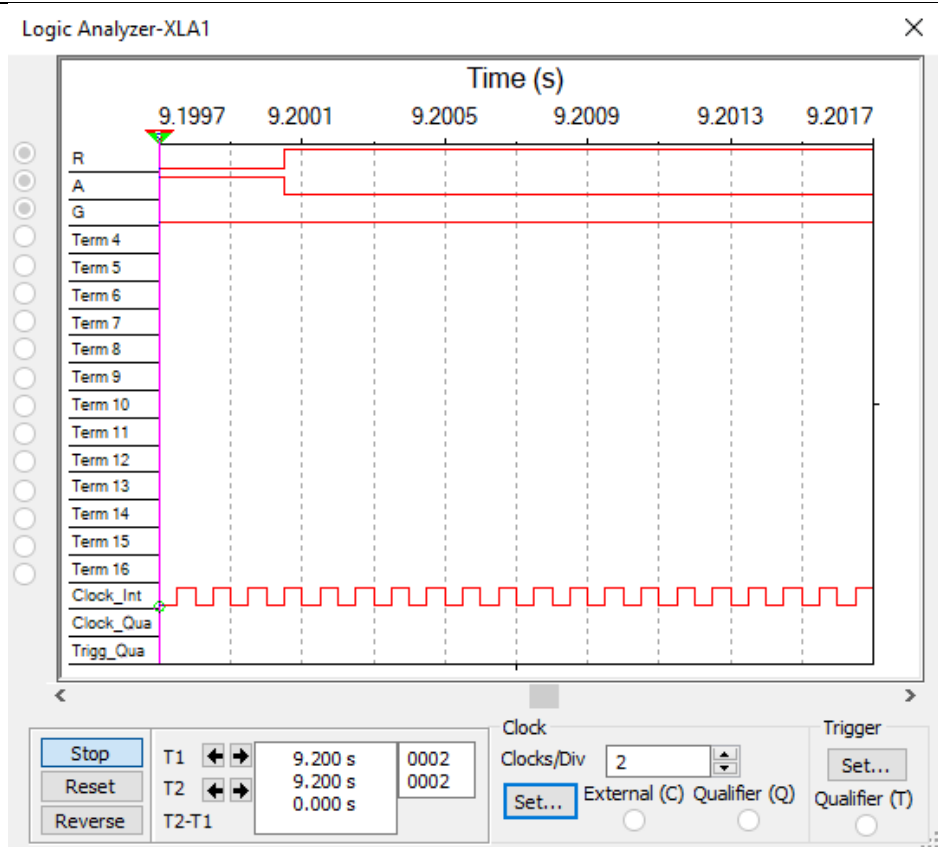


Fig 6.3

Traffic light analyser graph

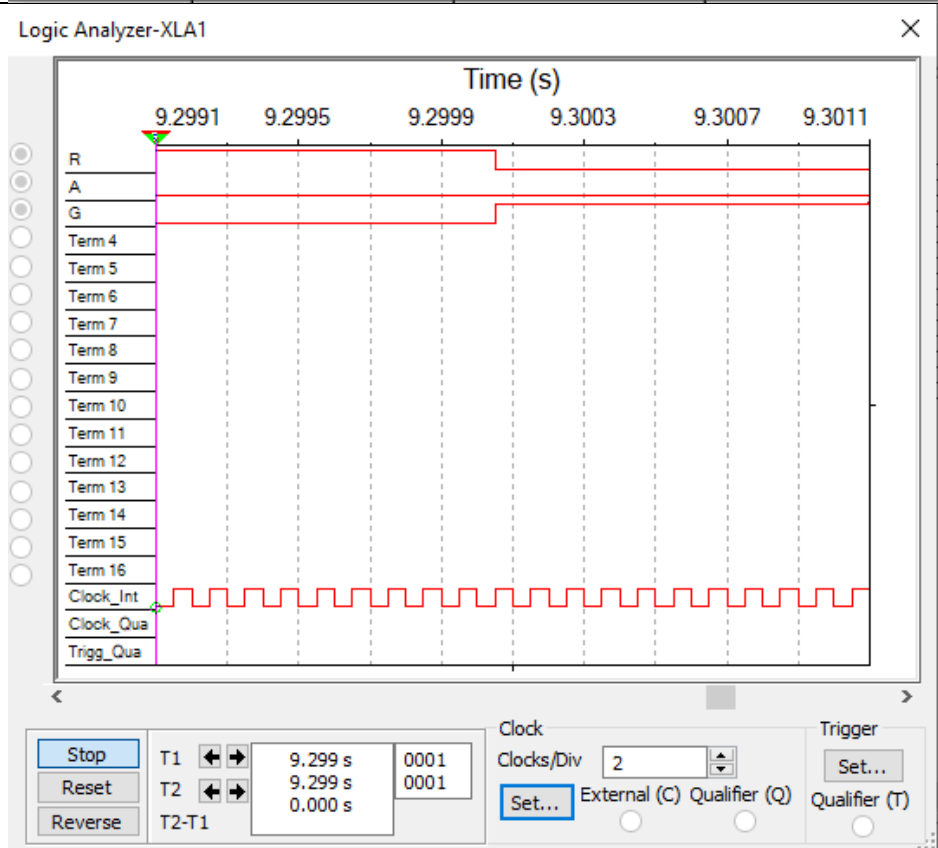


Fig 6.4

FINAL GRADE

GENERAL COMMENTS

Instructor

52/100

PAGE 1

PAGE 2

PAGE 3

PAGE 4

PAGE 5

PAGE 6

PAGE 7

PAGE 8

PAGE 9

PAGE 10

PAGE 11

PAGE 12

PAGE 13

PAGE 14

PAGE 15

PAGE 16

PAGE 17

PAGE 18

PAGE 19

PAGE 20

PAGE 21

PAGE 22

PAGE 23

PAGE 24

PAGE 25

PAGE 26

PAGE 27

PAGE 28

PAGE 29

GRADING FORM: CSG-RUBIC

JONATHAN DAVIES

52

RESEARCH-INFORMED LITERATURE



There was evidence of further reading and research with the inclusion of a reference list and appropriate in text referencing. Your interpretation and understanding of the additional research was good. Your references were appropriate to the task and your reference list was of an appropriate length for this assignment.

6

KNOWLEDGE AND UNDERSTANDING



The knowledge and understanding of the subject demonstrated by this assignment was reasonably detailed and mainly accurate. There were very few gaps in your knowledge of the basic concepts and your understanding of the higher level concepts was demonstrated to a limited degree - you could have explained in more detail how the circuit evolved. Further work – Your explanations need to be more detailed and written with a greater emphasis on critical evaluation rather than description.

14

ANALYSIS



Your explanation of the design process was good and the conclusions showed that you can interpret quantitative and qualitative data, although this was often descriptive. You could have evaluated the results and specified whether they concurred with theory suggesting reasons for any discrepancies. You have however demonstrated good analytical skills and your approach to the task was logical. Arguments made in the conclusions were mostly valid and demonstrated a good understanding of the topic. Further work – in your conclusion, you should relate the results to the original specification and to accepted theory.

14

PRACTICAL APPLICATION AND DEP.

12



Your application of practical skills for this task was generally adequate. You used the resources appropriately when designing the circuit and you used appropriate options for testing and evaluating the circuit performance. You managed to design a basic circuit that functioned within the specification and achieved this by only asking for assistance when appropriate thus demonstrating some basic problem solving skills. Your results were adequate and allowed for a reasonable conclusion to be attempted.

SKILLS FOR PROFESSIONAL PRAC.

6



In this assignment you have demonstrated skills in working individually and also collaboratively. Your written report was generally good and contained most of the required detail, it was also written in a coherent and logical way. The available word count was in the main effectively used.